IN THE CLAIMS

No claims have been amended herein.

1-9. (Canceled)

10. (Previously Presented) A software-driven emulation engine, comprising:

a plurality of clusters, each of said clusters including:

a data memory having a set of read ports and an operating clock rate for read operations; and

a plurality of processors that execute logic gate functions from a logic design, each of said processors having a set of read addresses and accessing said data memory, an operating clock rate of said processors differing from said operating clock rate of said data memory; and

a time division multiplexer associated with each of said clusters coupling said set of read ports of said data memory to said set of read addresses of one processor of said cluster during one read cycle of said data memory and coupling said set of read ports of said data memory to a set of read addresses of another processor of said cluster during the next read cycle of said data memory,

wherein said plurality of clusters and said time division multiplexer thereby verify a functionality of the logic design.

11. (Previously Presented) The software-driven emulation engine of claim 10, wherein said operating clock rate of said data memory is greater than said operating clock rate of said processors.

12. (Previously Presented) The software-driven emulation engine of claim 11, wherein said operating clock rate of said data memory is at least double said operating clock rate of said processors.

13. (Previously Presented) A software-driven emulation engine, comprising:

a plurality of clusters, each including:

a data memory having first and second sets of read ports and an operating clock rate; and

a plurality of processors for executing logic gate functions from a logic design, each of said processors of each of said clusters having a set of read addresses and accessing said data memory within each of said clusters, an operating clock rate of said processors differing from said operating clock rate of said data memory; and

a first time division multiplexer associated with each of said clusters that couples said first set of read ports of said data memory to said set of read addresses of a first processor of said cluster during one read cycle of said data memory and coupling said first set of read ports of said data memory to said set of read addresses of a second processor in said cluster during the next read cycle of said data memory; and

a second time division multiplexer associated with each of said clusters that couples said second set of read ports of said data memory to said set of read addresses of a third processor of said cluster during said one read cycle of said data memory and coupling said second set of read ports to said set of read addresses of a fourth processor in said cluster during said next read cycle of said data memory,

wherein said plurality of clusters, said first time division multiplexer, and said second time division multiplexer verify a functionality of the logic design.

14. (Previously Presented) The software-driven emulation engine of claim 13, wherein said operating clock rate of said data memory is operable during read operations.

15. (Previously Presented) The software-driven emulation engine of claim 13, wherein said operating clock rate of said data memory is greater than said operating clock rate of said processors.

16. (Previously Presented) The software-driven emulation engine of claim 15, wherein said operating clock rate of said data memory is at least double said operating clock rate of said processors.

17. (Previously Presented) An emulation engine, comprising:

a plurality of clusters, said clusters each comprising:

a data memory having a set of read ports and an operating clock rate; and

a plurality of processors for executing logic gate functions from a logic design, each of said processors within each of said clusters accessing said data memory within each of said clusters, an operating clock rate of said processors differing from said operating clock rate of said data memory; and

a time division multiplexer associated with each of said clusters coupling said set of read ports of said data memory to a set of read addresses of one processor within a first of said clusters during one read cycle of said data memory and coupling said set of read ports of said data memory to a set of read addresses of another processor within said first of said clusters during the next read cycle of said data memory,

wherein said plurality of clusters and said time division multiplexer verify a functionality of the logic design.

18. (Previously Presented) The emulation engine of claim 17, wherein said operating clock rate of said data memory is operable during read operations.

19. (Previously Presented) The emulation engine of claim 17, wherein said operating clock rate of said data memory is greater than said operating clock rate of said processors.

20. (Previously Presented) The emulation engine of claim 19, wherein said operating clock rate of said data memory is at least double said operating clock rate of said processors.